IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No 7,116,118 B2
Patent Issue Date ..... October 3, 2006
Application Serial No. 10/803,264
Filing Date ..... March 17, 2004
Assignee ..... Micron Technology, Inc.
Inventorship ..... Warren M. Farnworth et al.
Attorney's Docket No. MI22-2524
Title: Method and Apparatus for Testing Semiconductor Circuitry for Operability and Method of Forming Apparatus for Testing Semiconductor Circuitry for Operability

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR APPLICANT MISTAKES and PTO MISTAKES (37 C.F.R. §§ 1.322(a) and 1.323)

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTN: Decision and Certificate of Correction
Branch of the Patent Issue Division

From: D. Brent Kenady (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Sir:

It is hereby requested that a Certificate of Correction be issued with respect to Patent No. 7,116,118 B2, granted October 3, 2006, in accordance with the Certificate of Correction form attached hereto.

It is noted that errors appear in this patent of a typographical nature of character, as more fully described below. The errors occurred in good faith. Correction thereof does not involve such changes in the patent as would constitute new matter or would require re-examination.

The other error listed on the Certificate of Correction form were apparently incurred through the fault of the PTO as will be disclosed by the records of files in the Office.

Attached hereto, is Form PTO-1050, being suitable for printing.

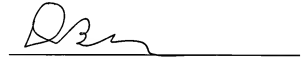
The exact page and line number where the errors occur in the application file are:

Page 11, line 13;

Page 13, line 18.

The Director is hereby authorized to charge the $100.00 fee as required under 37 CFR 1.20(a), or credit any overpayment, to Deposit Account No. 23-0925.

Respectfully submitted,

Dated: 7-18-07 By: 

D. Brent Kenady
Reg. No. 40,045

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,116,118 B2

DATED : October 3, 2006

INVENTOR(S) : Farnworth et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 4, line 26, please delete "s" after "such".

Col. 5, line 52, please delete "respect" after "atop" and insert --respective--.

Col. 6, line 48, please delete "apexes" after "conductive" and insert --apex--.

Mailing Address of Sender: D. Brent Kenady Wells St. John P.S. 601 West First Avenue, Suite 1300 Spokane, WA 99201-3828	Patent No. 7,116,118 B2